Digital I/O TTL and CMOS – TTL offers high switching speed and relative immunity to noisy systems. CMOS sensors provide image sensing technology by converting light waves into signals that are small bursts of current. These waves can be light or other electromagnetic radiation. NAI's TTL/CMOS Modules are offered in two versions: our Standard Functionality (SF) an Enhanced Functionality (EF) module. The transistor-transistor logic (TTL) employs transmitters with multiple emitters in gates having more than one input.

Module	Description
TL1	24 TTL Channels, Programmable I/O
TL2	24 TTL Channels, Enhanced, Programmable I/O

Features

- 24 channels available as inputs or outputs
- Programmable debounce circuitry with selectable time delay eliminates false signals resulting from relay contact bounce
- Built-in test runs in background constantly monitoring system health for each channel

Automatic Background Built-In Test (BIT)/Diagnostic Capability

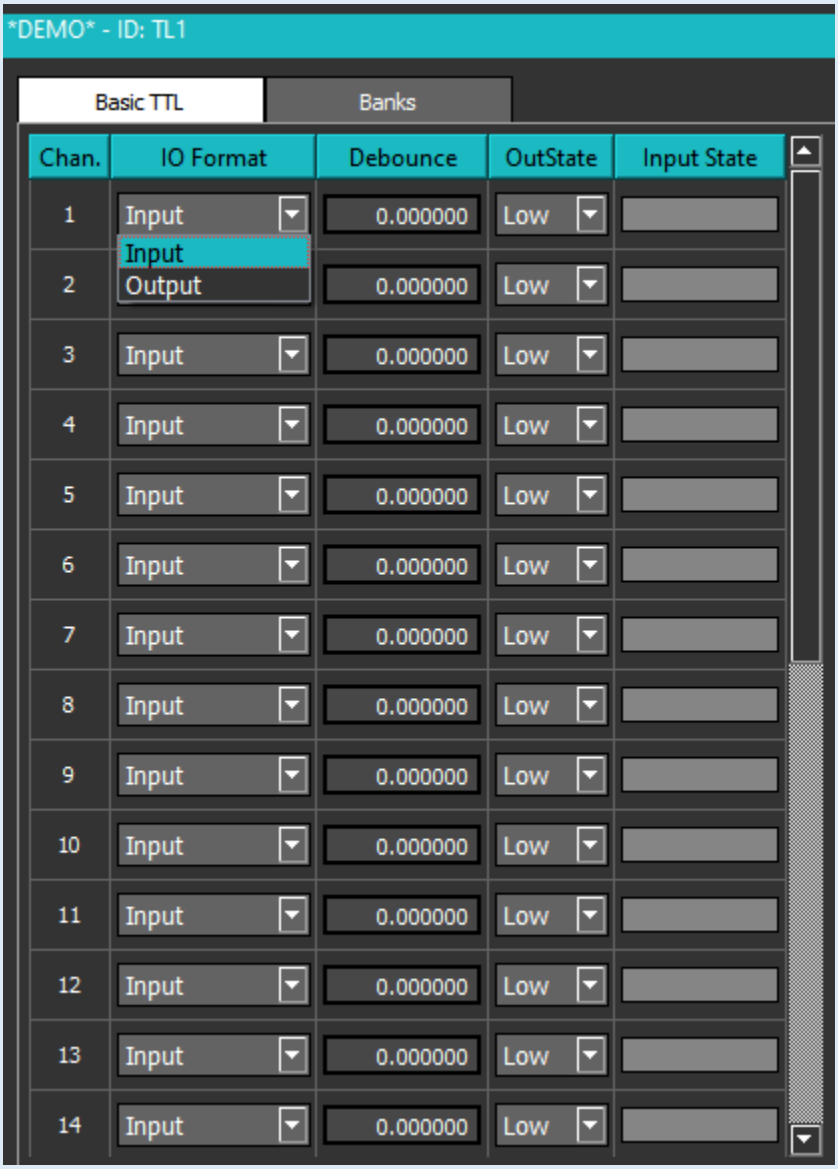
These modules contain automatic background BIT testing that verifies channel processing (data read or write logic), tests for overcurrent conditions and provides status for threshold signal transitioning. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each module. The test comparator checks each channel and is compared against the operational channel. Depending upon the configuration, the Input data read or Output logic written of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low-to-High and High-to-Low logic transitions are indicated.

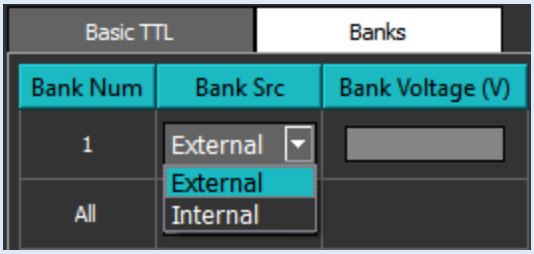
There is no independent overcurrent detection. Instead, the BIT detection circuitry is used to infer an overcurrent condition if the output state setting doesn't match the readback value seen by the input circuitry. For example, a shorted output, causing the read state to be opposite from the expected value would trigger this. If the fault persists beyond the BIT interval stabilization time, the overcurrent protection will kick in and reset the drive output by returning the transceiver to input mode. To reset this condition, a reset command needs to be issued to the Overcurrent Clear register, which will restore drive output and allow the latched status to be reset. This is separate from the reset for the Interrupt Enable Overcurrent register on this module. It is recommended that a reset command is done whenever status is cleared to avoid a non-apparent output reset condition

New Embedded Soft Panel

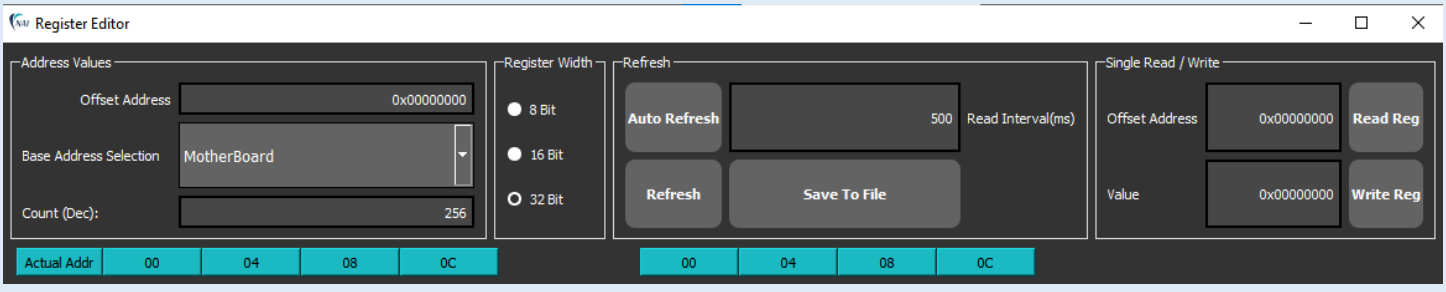
North Atlantic Industries offers the newest cross platform (Windows and Linux) GUI for our Gen 5 products that allows a user to quickly interact with our broad range of modular, I/O cards and rugged embedded computing products. Embedded Soft Panel 2 (ESP 2) is coherent and easy to use with a clean, fleshed out UI with features such as drag and drop dock able windows, a dark and light theme, and multi-language support. Multiple ways to open a board are offered, including saving board opening settings for future use. Interacting with and collecting information on hardware is simple to do with the register editor for reading and writing specific addresses, and the API logger which logs all API library calls including their return status and parameters. ESP 2 has many new features and provides an organized and effortless interface for NAI's next generation products. Available for CentOS 7.4 and 8.2 and Windows 10 x64

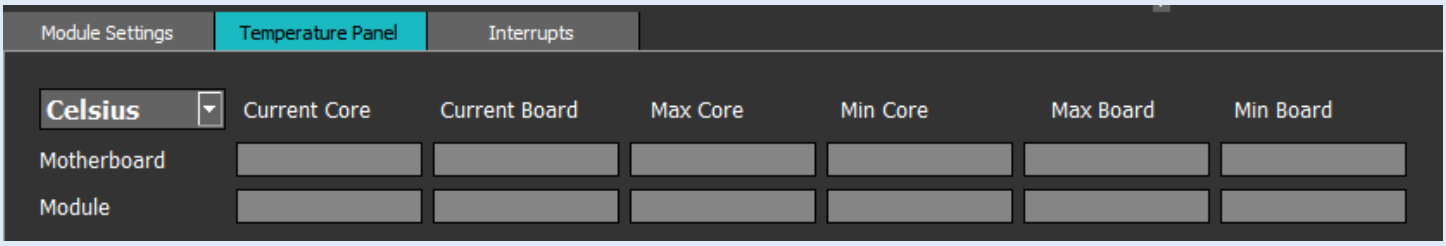
Digital I/O Example - Module TL1 Demo Mode Screen Shots

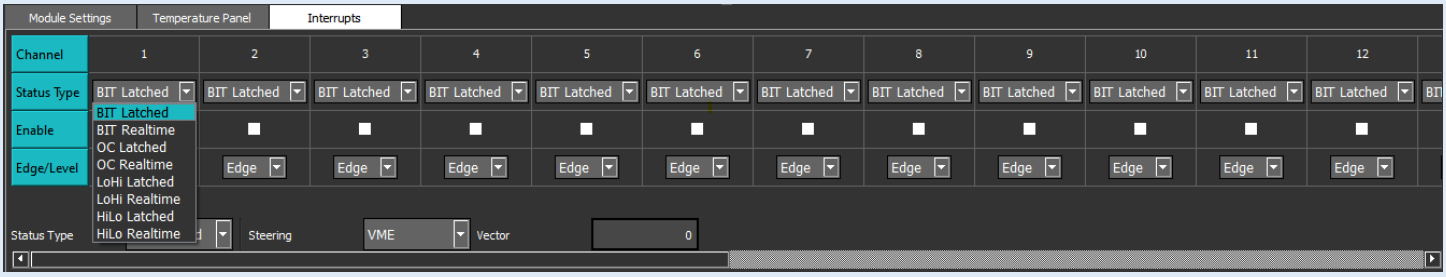



Basic TTL
Banks
Bank Num
Bank Src
Bank Voltage (V)
1
External
All
External
Internal


Status
Ch
BIT
OC
Lo ⇒ Hi
Hi ⇒ Lo
1
2
3
4
5
6
7
8
9
10
11
12
13
14
D L


Register Editor
Address Values
Offset Address
0x00000000
Base Address Selection
MotherBoard
Count (Dec):
256
Register Width
8 Bit
16 Bit
32 Bit
Refresh
Auto Refresh
500
Read Interval(ms)
Refresh
Save To File
Single Read / Write
Offset Address
0x00000000
Read Reg
Value
0x00000000
Write Reg
Actual Addr
00
04
08
0C
00
04
08
0C





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Rev. A